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**APPLICATION**  
**FOR**  
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**FOR:** A SYSTEM AND METHODOLOGY FOR  
CALCULATING THE COST OF FUTURE  
SEMICONDUCTOR PRODUCTS USING  
REGRESSION ANALYSIS OF HISTORICAL  
COST DATA

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**A SYSTEM AND METHODOLOGY FOR CALCULATING  
THE COST OF FUTURE SEMICONDUCTOR PRODUCTS  
USING REGRESSION ANALYSIS OF HISTORICAL COST DATA**

**BACKGROUND OF THE INVENTION**

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*Field of the Invention*

The present invention generally relates to cost prediction systems and more particularly to a novel system that predicts costs for future generations of technologies (for which the tooling and fabrication processes are unknown) based upon a regression analysis of current technologies.

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*Description of the Related Art*

Historical cost models look back in time at what has recently been run in a fabricator in order to compute "historical" (or actual) costs of products running in the fabricator. Historical cost models can even, to a degree, be enhanced to provide predictive cost data. However, the predictive capabilities of historical cost models are limited to products that are very similar to products currently running in the fabricator (such products are sometimes called "extensions" of current products). In the semiconductor art field, the gate dimension (e.g., gate

length in a transistor) is substantially the same for each technology generation. Therefore, a new technology generation (or simply "technology") is achieved when the gate dimension is reduced by a significant portion (e.g., greater than 10 %). An extension of a current technology will utilize the same gate dimension, but may include other enhancements not related to gate dimension.

Historical cost models have traditionally been less useful for costing future products that have much tighter specifications than the technology generation currently running in the fabricator. New processing techniques and tools are often required to achieve the next technology generation of gate dimension (i.e., smaller chip dimensions). Since many of these new techniques and tools do not yet exist in the fabricator, it is very difficult to accurately predict the cost of a wafer that will be running in the fabricator 1 to 5 years in the future.

At the same time, there is a desire in a highly competitive business environment to shrink groundrules and provide the next generation of technology as quickly as possible. Businesses are frequently asked to provide costs for products before they have the tools and techniques to produce them. Accurate predictive capability is required to make sound business case decisions regarding which products will be profitable now and in the future. Therefore, there is a need for a method and system that can predict the cost per wafer for future generations of technologies based solely upon historical data of known technologies.

## SUMMARY OF THE INVENTION

It is, therefore, an object of the present invention to provide a structure and method for predicting semiconductor product costs at a fabricator entailing a storage medium which includes a database of historical critical dimensions and historical critical groundrules correlated to cost functions at the fabricator. The user interface has user inputs for new design parameters and new critical groundrules associated with a new device to be produced at the fabricator and a computer adapted to receive the user inputs, extract data from the storage medium and compute semiconductor costs for the new device. The historical critical dimensions and the new critical dimensions are gate dimensions and the new critical dimensions are smaller than the historical critical dimensions. This device includes a future technology generation. Fabrication hardware and fabrication methods for producing the future technology generation are unknown and the relationships comprise base models and models that include options. The relationships comprise models that illustrate that costs increase exponentially as the historical critical dimensions and the historical critical groundrules are reduced.

The invention also comprises a method of predicting semiconductor product costs that performs a regression analysis on historical costs of historical critical dimensions at a fabricator, using the historical critical dimensions as independent variables and the historical costs as dependent variables. Where

creating, in a database, models from the regression analysis showing a relationship between the historical critical dimensions and the historical costs the invention inputs new design parameters and new critical dimensions of a new device into the database and predicts product costs of the new device based on the models.

A system embodiment of the invention for predicting semiconductor product costs at a fabricator includes a regression analyzer adapted to determine relationships between historical critical dimensions of historical technologies and costs of the historical technologies, a user interface for inputting a new critical dimension of a new technology and a calculator for predicting a cost of the new technology based on the new critical dimension and the relationships.

### **BRIEF DESCRIPTION OF THE DRAWINGS**

The foregoing and other objects, aspects and advantages will be better understood from the following detailed description of a preferred embodiment of the invention with reference to the drawings, in which:

Figure 1 is a graph illustrating the cost vs. critical gate dimension curve calculated with the invention;

Figure 2 is a chart illustrating the predicted cost vs. actual costs of different generations of technology;

Figure 3 is an exemplary worksheet used to predict cost for users of the

invention;

Figure 4 is a chart of equations for a technology cost estimate worksheet;

Figure 5 is a schematic diagram showing the overall technology cost

5 model overview; and

Figure 6 is a hardware implementation of the method of the invention.

## **DETAILED DESCRIPTION OF PREFERRED**

### **EMBODIMENTS OF THE INVENTION**

10 The invention solves the foregoing problem by extrapolating current costs of different technologies to future technologies. In other words, the invention looks at many different technology generations (e.g. 4th-9th generation of silicon-based technologies) and predicts the cost of future unknown generations (e.g., 10th or 11th generation of silicon-based technology). As mentioned above, in silicon-based technology, the generations are defined by relatively large  
15 reductions in the dimensions of the gate conductor in a transistor structure.

Therefore, the invention looks at historical costs for technologies producing different gate dimensions to predict the cost of future technologies that produce even smaller gate dimensions. No previous methodology or system calculates cost across different technology generations. Instead, conventional cost

prediction systems only predict cost within one technology generation (e.g., variations of a technology for a given gate dimension).

More specifically, the invention performs regression analysis on costs for all technologies currently running in a fabricator. In the examples shown in Figure 2 (discussed below), the 4th-9th generations of silicon processing are run in a fabricator.

The inventive regression analysis is performed by treating the lithography generation (or critical gate dimension) as the independent variable and wafer cost as the dependent variable. The invention produces a relationship curve such as the one illustrated in Figure 1. Thus, Figure 1 illustrates a power relationship between cost and technology generation (critical gate dimension lithographic groundrule). As can be seen from Figure 1, as the dimension of printed images of chip circuitry decreases (e.g., gate dimension decreases), cost increases exponentially as shown by the line 10 representing current costs and line 11 representing mature costs.

The regression analysis is actually performed in steps; one step for each section of semiconductor processing, with the results of all equations added together to form a composite equation.

Figure 1 is an example of relationships between technology critical dimension and costs for a particular semiconductor fabricator and can be used in conjunction with the worksheet shown in Figure 3 below (or any other similar

interface), by that semiconductor fabricator to project costs of future unknown technologies.

Thus, the invention enables the prediction of wafer processing cost before process flows even exist, indeed, even before the technology itself has been defined. As shown in Figure 2, the invention predicts cost within 7% - 10% of actual cost (e.g., % Delta). More specifically, Figure 2 illustrates the predicted and actual costs of two 4th generation technology (CM4L 3LM-which stands for CMOS 4th ("CM4") generation "L" with 3 last metalization ("3LM") layers; and CM4LP 3LM); four 5th generation technologies (CM5S 4LM, CM5S1 4LM, CM5X 4LM, and CM5X2 4LM); six 6th generation technologies (CM6S 4LM; CM6S2 4LM; CM6S2 5LM, CM6SF 4LM, CM6SF 5LM, CM6X 4LM, and SIGE6SF); two 7th generation technologies (CM7S 6LM and CM7SF 3LM); two 8th generation technology (CM8S 4LM and ICEC8S52 6LM); and a 9<sup>th</sup> generation technology (ICEC9S 7LM). As can be seen, the invention performs the prediction of future unknown technologies very well. The invention has been shown to predict future unknown technologies as well. For example, a predicted cost for 9<sup>th</sup> generation technology (CM9S 4LM) computed a year before the technology was introduced to the fabricator, yielded a predicted cost within 10 % of the actual cost.

It is possible for the invention to predict wafer processing costs before process flows exist and before the technology itself has been defined because of three main features of semiconductor processing. The first is that semiconductor



costs are largely driven by equipment, rather than materials or staffing. Second, while new equipment may be used in different or novel ways to achieve the new groundrules, new equipment is introduced each generation. Third, both of these things are especially true for photolithography and etch tools, which are the most critical tools toward achieving smaller dimensions. What these three features suggest, and what the invention relies upon, is that the cost of silicon-based semiconductors is predictive, even without knowing the specific processing or equipment parameters.

Referring now to Figure 3, a technology cost estimate worksheet is presented. The worksheet shown in Figure 3 is merely exemplary and, as would be known by a user of the invention, any similar input device or graphic user interface can be utilized to gather the information required to provide a cost estimate. Once information is obtained from the worksheet, the invention references the output of the regression analysis (e.g., Figure 1) to predict the future costs associated with a future technology.

In the first section of the worksheet 300, the technology 301 and photo groundrule 302 are input. The technology 301 can be a new technology or one of the technologies discussed above with respect to Figure 2 (e.g., CM4S). Additionally, the user indicates whether the technology is currently in production in item 303. A 'Y' would indicate that the estimate to be made is for an extension or variation of a known technology. An 'N' would indicate that the estimate to be made is for an unknown or new technology.

In section 310, the front-end of the processing line (FEOL) base cost is calculated. The front-end base processes include all semiconductor manufacturing steps up to and including the contact level, less optional levels. These processes are well known to those ordinarily skilled in the art and will not be discussed herein so as not to obscure the salient features of the invention. In item 313, the front-end base cost for different features (e.g., FEOL Base, BR Resistor) is calculated with the equations shown in Figure 4. Figure 4 shows the equation for the mature cost as well. Full capacity costs are based on the assumption of a full fabricator with some capacity held for development and inefficiency. The mature cost has no cycle time held. The equations shown in Figure 4 are merely an example of one fabricator and the invention is not limited to the exact equations shown therein. Instead, as would be known by one ordinarily skilled in the art, the equations for different fabricators will be different than those shown in Figure 4. The invention can apply a regression analysis to any historical data from any fabricator to arrive at the unique equations specific to that fabricator.

Also, in section 310 various options for the technology can be selected (column 311). The number of masks required for the dual gate option must be specified (item 312). In items 315 and 316 full capacity and mature costs are calculated using equations derived from the curves shown in Figure 1. In all cases, different process flows run in the fabricator were costed using a historical cost model. Least Squares Analysis performed on the points enabled the

generation of the general equations.

Item 317 and 318 are subtotals of the FEOL optional levels 315 and 316.

Items 319 and 320 represent the base cost 313, 314 and optional cost 319, 320  
5 combined.

In a similar manner, in section 370 the base costs of the back of the line  
(BEOL) processing (e.g.; processing that occurs after the cap layer is formed) 321,  
322 are calculated assuming four thin levels of metal and using the equation for  
the cost of a metal level shown in Figure 4.

10 In items 323 and 324, the user has the option of deleting various metal  
levels. These inputs are used to calculate the reduction in base cost shown as  
items 325 and 326. Again using the cost derived from the metal level equation  
shown in Figure 4.

15 In a similar manner, in items 327 and 328, the user can optionally add  
additional metal levels. In items 329 and 330, the costs of the additional levels is  
calculated using the equation shown in Figure 4.

Items 331 and 332 represent subtotals of the base cost 321, 322 having the  
deleted metal levels 325, 326 being removed or the additional metal levels 329,  
330 being added.

20 In item 333, the user can request copper wiring. Using the equation shown  
in Figure 4, the full capacity cost 334 and mature full capacity cost 335 for  
utilizing copper is calculated.

Item 336 allows the user to add an interconnect level (MC), a metal-insulator-metal capacitor (MIM) or TD level (required for high performance copper products) additional BEOL levels. Using the equation specified in Figure 4, items 337 and 338 provide the forecasted cost of such additional levels.

5           Items 339 and 340 represent a sum total of items 337 and 338. Item 341 is a summation of the previous subtotals 331, 334 and 339. Similarly, for the mature cost, item 342 represents a total of the subtotals 332, 335 and 340.

10           In section 390, the costs are summarized. More specifically for the full capacity cost, the base cost 313 and optional costs 317 are combined with a raw wafer cost 351 and super common processing 355. Super common processing includes all initial wafer treatments such as epi deposition (if raw wafers do not include it), initial wafer clean, and nitride and polysilicon deposition. If the technology is not currently in production, a contingency of 10% is added in item 357. Items 355 and 357 are then summarized in item 359 to derive a total  
15           projected cost.

20           In a similar manner, for the mature full capacity cost, the base cost 314 is added to the optional cost 318, the raw wafer cost 352, and the super common 354. Once again a subtotal appears in item 356. Also, 10% 358 is added if the technology is not currently in production. Items 356 and 358 are then  
20           summarized in item 360 to produce the total predicted cost for the mature for capacity.

Referring now to Figure 5, a system embodiment of the invention is

illustrated. More specifically, Figure 5 illustrates a regression analyzer 41 which performs least-square-analysis (also known as regression analysis) on historical data 40 from many different technology generations to create the critical dimensions/cost relationship discussed above. The critical dimensions/cost relationship can be stored, for example, in a database 42. A calculator or computer can be utilized as the cost prediction unit 44 which takes user input regarding a new technology through any user interface 43 (such as the interface shown in Figure 3) and calculates the cost prediction for the new technology 45 based upon the critical dimensions/cost relationship 42.

While the overall methodology of the invention is described above, the invention can be embodied in any number of different types of systems and executed in any number of different ways, as would be known by one ordinarily skilled in the art. For example, as illustrated in Figure 6, a typical hardware configuration of an information handling/computer system in accordance with the invention preferably has at least one processor or central processing unit (CPU) 500. For example, the central processing unit 500 could include various weighting units, classification units, clustering units, filters, adders, subtractors, comparators, etc. Alternatively, as would be known by one ordinarily skilled in the art given this disclosure, multiple specialized CPU's (or other similar individual functional units) could perform the same processing, weighting, classifying, clustering, filtering, adding, subtracting, comparing, etc.

The CPU 500 is interconnected via a system bus 501 to a random access

memory (RAM) 502, read-only memory (ROM) 503, input/output (I/O) adapter 504 (for connecting peripheral devices such as disk units 505 and tape drives 506 to the bus 501), communication adapter 507 (for connecting an information handling system to a data processing network) user interface adapter 508 (for connecting peripherals 509-510 such as a keyboard, mouse, imager, microphone, speaker and/or other interface device to the bus 501), a printer 511, and display adapter 512 (for connecting the bus 501 to a display device 513). The invention could be implemented using the structure shown in Figure 6 by including the inventive method, described above, within a computer program stored on the storage device 505. Such a computer program would act on a information supplied through the interface units 509-510 or through the network connection 507. The system would then automatically perform the processing discussed above and produce an output on the display 513, through the printer 511 or back to the network 507.

The benefits of this model are that they allow interpolation and extrapolation of existing cost data to predict future cost data. This is especially useful in a manufacturing environment where future products are manufactured from the same basic raw materials processing principles, but can be made with different features, or, future products that are improved performance versions of current products. Outside the manufacturing environment, these same principles could be applied to any costing effort where costs are, 1) known (a historical database exists), and, 2) the critical parameters that drive cost are known or can be

derived. In that case, regression analysis can be used and a user interface created to enable the prediction of future products.

While the invention has been described in terms of preferred embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.

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